**Lesson Plan**

**Name of Faculty : Sh. Paritosh Parashar**
**Discipline : ECE**
**Semester : 3rd**
**Subject : Digital Electronics**
**Lesson Plan Duration : 16 weeks**
**Work load (Lecture /Practical) per week (in hours): Lectures—03, Practical—04**

| Week | Theory | | Practical | |
|---|---|---|---|---|
| | Lecture Day | Topic (Including Assignment/ Test | Practical Day | Topic |
| 1st | 1 | Introduction | 1st | Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR (EXNOR) gates |
| | 2 | Distinction between analog and digital signal. | | |
| | 3 | Applications and advantages of digital signals | | |
| 2nd | 4 | Assignment | 2nd | Realisation of logic functions with the help of NAND or NOR gates |
| | 5 | Binary | | |
| | 6 | octal and hexadecimal number system | | |
| 3rd | 7 | conversion from decimal and hexadecimal to binary and vice-versa | 3rd | To design a half adder using XOR and NAND gates and verification of its operation |
| | 8 | Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction. | | |
| | 9 | Assignment | | |
| 4th | 10 | Concept of code, weighted and non-weighte codes | 4th | To design of a full adder circuit using XOR and NAND gates and verify its operation |
| | 11 | examples of 8421, BCD, excess-3 and Gray code | | |
| | 12 | Concept of parity, single and double parity and error detection | | |
| 5th | 13 | Assignment | 5th | To design circuit for 7 segment display ICs |
| | 14 | Concept of negative and positive logic | | |
| | 15 | Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR, EXOR Gates | | |
| 6th | 16 | NAND and NOR as universal gates | 6th | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops). |
| | 17 | Introduction to TTL and CMOS logic families | | |
| | 18 | Assignment | | |
| 7th | 19 | Logic Simplification | 7th | Verification of truth table for positive edge triggered, negative edge triggered, level |
| | 20 | Postulates of Boolean algebra, De Morgan's Theorems | | |
| | 21 | Implementation of Boolean (logic) equation | | |

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|---|---|---|---|---|
| | | with gates | | triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops). |
| 8th | 22 | Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits | 8th | Verification of truth table for encoder and decoder ICs |
| | 23 | Half adder and Full adder circuit | | |
| | 24 | design and implementation | | |
| 9th | 25 | 4 bit adder circuit | 9th | Verification of truth table for Multiplexers and x and De-Multiplexers |
| | 26 | Decoders, Multiplexers, Multiplexers and Encoder | | |
| | 27 | Four bit decoder circuits for 7 segment display and decoder/driver ICs | | |
| 10th | 28 | Basic functions and block diagram of MUX and DEMUX with different ICs | 10th | To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation |
| | 29 | Basic functions and block diagram of Encoder | | |
| | 30 | Concept and types of latch with their working and applications | | |
| 11th | 31 | Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops | 11th | To design a 4 bit ring counter and verify its operation. |
| | 32 | Difference between a latch and a flip flop | | |
| | 33 | Introduction to Asynchronous and Synchronous counters | | |
| 12th | 34 | Binary counters | 12th | Use of Asynchronous Counter ICs (7490 or 7493) |
| | 35 | Divide by N ripple counters | | |
| | 36 | Decade counter | | |
| 13th | 37 | Ring counter | 13th | To design and verification of A/D converter |
| | 38 | Assignment | | |
| | 39 | Introduction and basic concepts including shift left and shift right | | |
| 14th | 40 | serial in serial out, parallel in serial out parallel in parallel out parallel in parallel out Universal shift register | 14th | To design and verification of D/A converter |
| | 41 | Working principle of A/D and D/A converters | | |
| | 42 | Stair step Ramp A/D converter, Dual Slope A/D converter | | |
| 15th | 43 | Successive Approximation A/D Converter | 15th | To design and verification of 74181 ALU IC |
| | 44 | Binary Weighted D/A converter | | |
| | 45 | R/2R ladder D/A converter, Applications of A/D and D/A converter | | |
| 16th | 46 | Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, and EEPROM) | 16th | Revision of Experiments |
| | 47 | static and dynamic RAM | | |
| | 48 | introduction to 74181 ALU IC | | |