

## Lesson Plan

Name of Faculty : Bharti  
 Discipline : ECE  
 Semester : 3<sup>rd</sup> Semester  
 Subject : Digital Electronics  
 Lesson Plan Duration : 16 weeks  
 Work Load per week{ in hours) : Lectures-03, Practical-04

| Week | Theory      |                                                                                              |               | Practical                                                                                       |
|------|-------------|----------------------------------------------------------------------------------------------|---------------|-------------------------------------------------------------------------------------------------|
|      | Lecture Day | Topic                                                                                        | Practical day | Topic                                                                                           |
| 1st  | 1           | Introduction to analog and digital signal                                                    | 1st           | Verification and interpretation of truth tables for AND,OR, NOT, NAND,NOR ,EXOR and EXNOR gates |
|      | 2           | Binary,Octal number System                                                                   |               |                                                                                                 |
|      | 3           | Hexa Decimal number system, Conversion from Decimal and hexadecimal to binary and vice-versa |               |                                                                                                 |
| 2nd  | 4           | Conversion of number system                                                                  | 2nd           | Realisation of logic function with the help of NAND or NOR gates                                |
|      | 5           | Binary addition and Subtraction including binary points                                      |               |                                                                                                 |
|      | 6           | 1's and 2's complement method of addition and subtraction.                                   |               |                                                                                                 |
| 3rd  | 7           | Concept of code, weighted and non weighted codes                                             | 3rd           | To design half adder using XOR and NAND gates and verification of its operation                 |
|      | 8           | Example 8421, BCD, Excess-3 and gray code                                                    |               |                                                                                                 |
|      | 9           | Concept of parity, Single and Double parity, Error Detection                                 |               |                                                                                                 |
| 4th  | 10          | Concept of negative and positive logic                                                       | 4th           | To design full adder using XOR and NAND gates and verification of its operation                 |
|      | 11          | Definition , Symbol and truth tables of Not,AND,OR gate                                      |               |                                                                                                 |
|      | 12          | Definition , Symbol and truth tables of NAND,NOR,EXOR gates                                  |               |                                                                                                 |
| 5th  | 13          | NAND and NOR as universal gates                                                              | 5th           | To design circuit for 7 segment display ICs.                                                    |
|      | 14          | Introduction to TTL and CMOS logic families                                                  |               |                                                                                                 |
|      | 15          | Postulates of Boolean algebra,                                                               |               |                                                                                                 |
| 6th  | 16          | De morgan's theorems, Implementation of Boolean                                              | 5th           | To design circuit for 7 segment display ICs.                                                    |
|      | 17          | Karnaugh map(upto 4 variables) and simple applications of developing combinational circuits  |               |                                                                                                 |
|      | 18          | Half Adder , Full Adder circuit, Design and implementation                                   |               |                                                                                                 |
| 7th  | 19          | 4-bit adder circuit                                                                          | 6th           | Verification of truth table for positive edge triggered, negative                               |
|      | 20          | Four bit Decoder circuits for 7 segment display and decoder /driver ICs                      |               |                                                                                                 |

|      |    |                                                                           |                                            |                                                                                                                                                                                |
|------|----|---------------------------------------------------------------------------|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | 21 | Basic function and block diagram of MUX and DEMUX with different ICs      |                                            | edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops).                                                                   |
| 8th  | 22 | Basic function and block diagram of Encoder                               | 6th                                        | Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip-flops). |
|      | 23 | Concept and types of Latch with their working and application             |                                            |                                                                                                                                                                                |
|      | 24 | Operation using waveforms and truth-table of RS, T flip-flops             |                                            |                                                                                                                                                                                |
| 9th  | 25 | Operation using waveforms and truth-table of D,Master/Slave JK flip-flops | 7th                                        | Verification of truth table for encoder and decoder ICs.                                                                                                                       |
|      | 26 | Difference between a latch and a flip-flop                                |                                            |                                                                                                                                                                                |
|      | 27 | Introduction to Asynchronous and Synchronous counters, Binary counters    |                                            |                                                                                                                                                                                |
| 10th | 28 | Divide by N ripple counters, Decade counter ,Ring Counter                 | 8th                                        | Verification of truth table for Multiplexers and x and De-Multiplexers                                                                                                         |
|      | 29 | Introduction and basic concepts including shift left and shift right      |                                            |                                                                                                                                                                                |
|      | 30 | SIPO,SISO,PISO,PIPO                                                       |                                            |                                                                                                                                                                                |
| 11th | 31 | Universal shift register                                                  | 9th                                        | To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.                                                            |
|      | 32 | Working Principle of A/D and D/A converters                               |                                            |                                                                                                                                                                                |
|      | 33 | Stair step Ramp A/D converter                                             |                                            |                                                                                                                                                                                |
| 12th | 34 | Dual Slope A/D converter                                                  | 10th                                       | To design a 4 bit ring counter and verify its operation.                                                                                                                       |
|      | 35 | Successive Approximation A/D converter                                    |                                            |                                                                                                                                                                                |
|      | 36 | Binary Weighted D/A converter                                             |                                            |                                                                                                                                                                                |
| 13th | 37 | R/2R Ladder D/A converter                                                 | 11th                                       | Use of Asynchronous Counter ICs (7490 or 7493)                                                                                                                                 |
|      | 38 | Application of A/D and D/A converter                                      |                                            |                                                                                                                                                                                |
|      | 39 | Memory Organization , Classification of Semiconductor memories            |                                            |                                                                                                                                                                                |
| 14th | 40 | RAM,ROM,PROM                                                              | 12th                                       | To design and verification of A/D converter                                                                                                                                    |
|      | 41 | EPROM,EEPROM                                                              |                                            |                                                                                                                                                                                |
|      | 42 | Static and dynamic RAM                                                    |                                            |                                                                                                                                                                                |
| 15th | 43 | Introduction to 74181 ALU IC                                              | 13th                                       | To design and verification of D/A converter                                                                                                                                    |
|      | 44 | Revision                                                                  |                                            |                                                                                                                                                                                |
|      | 45 |                                                                           |                                            |                                                                                                                                                                                |
| 16th | 46 | 14th                                                                      | To design and verification of 74181 ALU IC |                                                                                                                                                                                |
|      | 47 |                                                                           |                                            |                                                                                                                                                                                |
|      | 48 |                                                                           |                                            |                                                                                                                                                                                |